REMARKS

Claims 1-37 are pending. Claims 1-3, 6-9, 16, 19, 22-26, 33-34, and 37 are rejected under 35 U.S.C. § 103(a). Claims 4-5, 10-15, 17-18, 20-21, 27-32, and 35-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

Independent claims 1, 16, 25, and 37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Robertson et al. in view of Wei (U.S. Pat. No. 6,473,878) and further in view of Ko (U.S. Pat. No. 6,473,878). Claim 1 recites "a first mapper coupled to said first input for applying a first coded bits-to-signal mapping to said **coded bits** to produce a first output signal; a second mapper coupled to said second input for applying a second coded bits-to-signal mapping to the **interleaved version of said coded bits** to produce a second output signal, **wherein said second coded bits-to-signal mapping differs from said first coded bits-to-signal mapping.**"

Claim 16 recites "a first mapper coupled to said first coder for applying a first coded bits-to-signal mapping to said **coded bits** to produce a first output signal; and a second mapper coupled to said second coder for applying a second coded bits-to-signal mapping to the **interleaved version of said coded bits** to produce a second output signal, **wherein said second coded bits-to-signal mapping differs from said first coded bits-to-signal mapping.**"

Claim 25 recites "applying a first coded bits-to-signal mapping to said **coded bits** to produce a first output signal; applying a second coded bits-to-signal mapping to the **interleaved version of said coded bits** to produce a second output signal, **wherein said second coded bits-to-signal mapping differs from said first coded bits-to-signal mapping.**"

Claim 34 recites "applying a first coded bits-to-signal mapping to said **coded bits** to produce a first output signal; and applying a second coded bits-to-signal mapping to the

interleaved version of said coded bits to produce a second output signal, **wherein said second coded bits-to-signal mapping differs from said first coded bits-to-signal mapping.**"

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. (MPEP § 2143). Applicant respectfully submits that Examiner has failed to establish all three criteria. Thus, claims 1-3, 6-9, 16, 19, 22-26, 33-34, and 37 are patentable under 35 U.S.C. § 103(a) over Robertson et al. in view of Wei and further in view of Ko.

Applicants hereby reiterate their previous argument in their response dated June 27, 2005, with regard to claims 1-3, 6-9, 16, 19, 22-26, 33-34, and 37. Examiner has failed to show that Robertson discloses different mappers or different mapping as required by each of independent claims 1, 16, 25, and 34. Examiner now states that Ko discloses teaches different mappings in Figure 5 with mappers 23 and 24 being different. (Office Action dated 9/20/2005, paragraph 24). The different mappers of Figure 5, however, receive completely different bits. Referring to column 6, lines 15-20, Ko discloses the use of three 3-to-2 mappers and one 5-to-3 mapper, because 14 input bits are mapped to 9 output bits. For example, 3+3+3+5 = 14 input bits and 2+2+2+3 = 9 output bits. Claim 1, however, recites "applying a first coded bits-to-signal mapping to said coded bits to produce a first output signal" and "applying a second coded bits-to-signal mapping to the interleaved version of said coded bits." One mapping, therefore, is applied to the coded bits and another mapping is applied to an interleaved version of the same coded bits. No combination of Robertson, Wei, or Ko disclose these limitations. Moreover, since similar emphasized limitations are also included in each of independent claims 16, 25, and 34, applicants respectfully submit that claims 1-3, 6-9, 16, 19, 22-26, 33-34, and 37 are patentable under 35 U.S.C. § 103(a) over the cited references.

Furthermore, one of ordinary skill in the art at the time of the present invention would not think to combine Ko with Robertson and Wei. Apart from Examiner's improper hindsight, there is nothing to suggest that Ko would use different mappers in Figure 5 if the number of input bits was an integral multiple of three. In fact, Ko specifically discloses using exactly the same mappers at Figures 2 and 4 where there are 12 input bits.

Examiner states that "the combined teaching of Robertson and Ko suggest different mappings as recited by the instant claims." (Office Action dated 9/20/2005, paragraph 14). Applicants respectfully disagree. Robertson discloses two signal mappers at Figure 1. Examiner even admits "Robertson broadly shows two signal mappers without indicating whether or not they are the same." (Office Action dated 9/20/2005, paragraph 8). Examiner relies on Figure 5 of Ko for the disclosure of different mappers. As previously discussed, however, these mappers operate on completely different input data. There is no teaching or suggestion in either reference that would motivate one of ordinary skill in the art to combine Robertson with Ko to produce the claimed invention. Thus, claims 1-3, 6-9, 16, 19, 22-26, 33-34, and 37 are patentable under 35 U.S.C. § 103(a) over the cited references.

Examiner further states that "Ko suggests the beneficial use of separate signal mappers being different such as changing the code length (i.e. changing constellation size which would change the number of bits per symbol) for transmission according to conditions and also to accommodate the memory size (Ko col. 1 lines 10-15) in the analogous art of signal mapping." (Office Action dated 9/20/2005, paragraph 14). Applicants have repeated column 1, lines 6-15 for Examiner's reference.

> The present invention relates to an apparatus for encoding and decoding run length limited (RLL) code data, and more particularly to an encoding and decoding apparatus for modulating input data by encoding the input data to run length limited (RLL) code data and decoding the modulated RLL code data, in which the transmission code length is shortened according to the minimum run length condition so that the memory size required for encoding and decoding RLL code data can be reduced.

Examiner will note there is nothing in the foregoing paragraph even remotely related to the beneficial use of separate signal mappers or different signal mappers. Moreover, it is completely irrelevant to the invention of claims 1-3, 6-9, 16, 19, 22-26, 33-34, and 37. Applicants request clarification. Did Examiner mistakenly cite the wrong paragraph?

In view of the foregoing, applicants respectfully request reconsideration and allowance of claims 1-37. If the Examiner finds any issue that is unresolved, please call applicants' attorney by dialing the telephone number printed below.

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